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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,251	09/25/2003	David F. Hepner	SJO920030029US1	5963

7590 08/21/2008

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EXAMINER	
DU, THUAN N	
ART UNIT	PAPER NUMBER
2116	
MAIL DATE	DELIVERY MODE
08/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,251	HEPNER ET AL.	
	Examiner	Art Unit	
	Thuan N. Du	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Appeal Brief (dated 6/30/2008).

2. In view of the appeal brief filed on 6/30/2008, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Rehana Perveen/

Supervisory Patent Examiner, Art Unit 2116

3. Claims 1-20 are presented for examination.

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-4 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Circenis, U.S. Patent No. 6,816,809 in view of Chakravarthy et al [Chakravarthy], U.S. Pub. No. 2004/0059956.

6. As per claim 1, Circenis teaches a system comprising a CPU (210-213), a clock (system clock 230), a counter (240-243) counting clock pulse to the CPU, wherein the clock is adapted to provide a CLK to the counter when a software task is running on the CPU [Fig. 3; col. 3, line 61 to col. 4, line 3; col. 5, line 66 to col. 6, line 9; col. 3, lines 24-25], said counter adapted to count number of clock pulses since a reset [col. 7, lines 17-21]; the CPU adapted to provide a RESET signal (signal preventing incrementing of the counter values) to the counter for each CLK pulse when a software task is not running on the CPU (CPU provides idle indication to counter via indicator 220-223) [col. 7, lines 12-17, 21-25]; and means for storing the counter value [col. 3, lines 45-46; col. 6, lines 4-6, 10-11].

Circenis does not explicitly teach the clock providing clock signal to the CPU. However, one of ordinary skill in the art would have recognized that the CPU must receive a clock signal (i.e. derives from system clock) to operate the CPU. Circenis also does not explicitly teach a monitor adapted to store the value in the counter immediately prior to the last RESET.

Chakravarthy teaches a microprocessor system comprising a CPU (120), a clock (PLL 208) providing a CLK signal to the CPU [paragraph 21, lines 5-7], a counter (within

performance monitor 204) counting clock pulses to the CPU [paragraph 28, lines 1-4], and a monitor (performance monitor 204), wherein the clock (208) is adapted to provide a CLK signal to the counter (via 210) when a software task is running on the CPU [paragraph 28]; and the monitor is adapted to store the value in the counter immediately prior to the last RESET (Chakravarthy saving the counted clock pulses as "Time0" when a CPU_CLKS UNHALTED event occurs) [paragraph 36].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Circenis to store the value in the counter immediately prior to the last RESET as taught by Chakravarthy because it would increase the reliability of the system.

7. As per claim 2, Circenis discloses the microprocessor system wherein the CPU is adapted to block a RESET signal to the counter when a software task is running on the CPU (when CPU is running, the counter value is incremented) [col. 7, lines 17-21].

8. As per claim 3, Chakravarthy discloses the CPU is adapted to continuously pass CLK signals (via 210) to the counter when a software task is running on the CPU [paragraphs 27 and 28].

9. As per claim 4, Circenis discloses the microprocessor system wherein the CPU is adapted to pass a RESET signal to the counter when is software task is not running on the CPU [col. 7, lines 12-17, 21-25].

10. As per claims 11-14, they do not teach or further define over the limitations recited in the rejected claims above. Therefore, claims 11-14 are also rejected as being

unpatentable over Circenis in view of Chakravarthy for the same reasons set forth in the rejected claims above.

11. Claims 5-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Circenis, U.S. Patent No. 6,816,809 in view of Chakravarthy et al [Chakravarthy], U.S. Pub. No. 2004/0059956 and further in view of Terrell, II [Terrell], U.S. Pub. No. 2004/0098631.

12. As per claims 5 and 15, Circenis-Chakravarthy does not disclose the monitor of the microprocessor system is adapted to output a control signal responsive to monitor content. Terrell teaches a system clock power management system wherein a clock controller (10 or 62) is adapted to output control signals (14) to processors within the system (20 and 24 or 50 and 52) to control the common clock to the processors dependent on processor usage and clock counts when processor is active (paragraphs 15 and 32). It would have been obvious to one of ordinary skill of the art having the teachings of Circenis-Chakravarthy and Terrell, at the time the invention was made to modify the performance monitor of Circenis-Chakravarthy to include the ability to send control signals in response to monitored activity as taught by Terrell. One of ordinary skill in the art would be motivated to make this combination in order to give the ability of the performance monitor to output control signals in view of the teachings of Terrell, as doing so would give the added benefit of monitoring both common and shared processor clock usage between multiple processors instead of one [paragraphs 9 and 10].

13. As per claims 6 and 16, Terrell teaches the microprocessor system wherein the monitor is adapted to output a power control signal responsive to monitor content (controlling the clock frequency to the processing elements thus controlling power) [paragraph 15].

14. As per claims 7 and 17, Terrell teaches the monitor is adapted to output a function control signal responsive to monitor content (the output control signals from the monitor circuit (clock controller) are in response to hardware interrupts received from the system) [paragraph 46].

15. As per claims 8 and 18, Terrell teaches the monitor is adapted to output a clock control signal responsive to monitor content (controlling the clock frequency to the processing elements thus controlling power) [paragraph 15].

16. As per claims 9 and 19, Terrell teaches the monitor is adapted to output a control signal reducing power input to the CPU responsive to monitor content when tile monitor content is below a threshold ("guard band" frequency) [paragraphs 13 and 53].

17. As per claims 10 and 20, Terrell teaches the monitor is adapted to output a control signal reducing clock pulse input to the CPU responsive to count content when the monitor content is below a threshold [paragraph 53].

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday-Friday: 7:30 AM - 4:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571) 272-3676.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

TD
August 18, 2008

/Thuan N. Du/
Primary Examiner, Art Unit 2116